SIS - Simple Instruction Simulator

for version 2.17, 31 May 2019

Jiri Gaisler (jiri@gaisler.se)

This manual is for SIS (version 2.17, 31 May 2019).

Table of Contents

1 Introduction . . . 1

2 Invoking sis . . . 2

3 Commands . . . 3

4 Emulated Systems . . . 6

4.1 ERC32 SPARC V7 processor . . . 6
4.1.1 IU and FPU instruction timing. . . . 6
4.1.2 UART A and B . . . 7
4.1.3 Real-time clock and general purpose timer A . . . 8
4.1.4 Interrupt controller . . . 8
4.1.5 System fault status registers . . . 8
4.1.6 Memory interface . . . 8
4.1.7 Watchdog . . . 9
4.1.8 Software reset register . . . 9
4.1.9 Power-down mode . . . 9
4.1.10 MEC control register . . . 9
4.2 LEON2 emulation . . . 9
4.2.1 LEON2 peripherals . . . 10
4.2.2 Memory interface . . . 10
4.2.3 Power-down mode . . . 10
4.3 LEON3 emulation . . . 10
4.3.1 LEON3 peripherals . . . 10
4.3.2 Memory interface . . . 10
4.3.3 Power-down mode . . . 11
4.4 RISC-V emulation . . . 11
4.4.1 Power-down mode . . . 11
4.4.2 Code coverage . . . 11
4.4.3 RISC-V 64-bit timer . . . 11

5 Multi-processing . . . 12

6 Interfacing to GDB . . . 13

7 Code coverage . . . 14

8 Building SIS . . . 15

Appendix A GNU Free Documentation License **16**

Index **24**

1 Introduction

SIS is a SPARC V7/V8 and RISC-V RV32IMACFD architecture simulator. It consist of three main parts: an event-based simulator core, a cpu (SPARC/RISCV) emulation module and system-specific memory and peripheral modules.

SIS can emulate four specific systems:

`ERC32` ERC32 SPARC V7 processor

`LEON2` LEON2 SPARC V8 processor

`LEON3` LEON3 SPARC V8 processor

`RISC-V` RISC-V (RV32IMACFD) processor

The LEON3 and RISC-V emulation also supports SMP with up to four processor cores.

2 Invoking sis

The simulator is started as follows:

```
sis [options] [file]
```

The following options are recognized:

`-c` *`file`* Read sis commands from *file* at startup.

`-cov` Enable code coverage and write a coverage file at exit.

`-d` *`clocks`* Set the the number of *clocks* in each time-slice for multi-processor simulation. Default is 50, set lower for higher accuracy.

`-erc32` Emulate the SPARC V7 ERC32 processor

`-freq` *`freq`*
Set frequency of emulated cpu. This is used by the 'perf' command to calculated the MIPS figure for a particular configuration. The frequency must be an integer indicating the frequency in MHz.

`-gdb` Start a gdb server, listening on port 1234. An alternative port can be specified with *-port nn*.

`-leon2` Emulate the SPARC V8 LEON2 processor

`-leon3` Emulate the SPARC V8 LEON3 processor

`-m` *`cores`* Enable the number of *cores* (2 - 4) in a leon3 or RISC-V multi-processor system.

`-nfp` Disable the simulated FPU, so each FPU instruction will generate a FPU disabled trap.

`-port` *`port`*
Use *port* for the gdb server. Default is port 1234.

`-r` Start execution immediately without an interactive shell. This is useful for automated testing.

`-riscv` Emulate a RISC-V RV32IMACFD processor

`-tlim` *`delay`*
Used together with *-r* to limit the amount of simulated time that the simulator runs for before exiting. The following units are recognized: *us*, *ms* and *s*. To limit simulated time to 100 seconds, use: *-tlim 100 s*.

`-uart1` *`device`*
Connect UART1 (console) of the simulator to *device*. stdin/stout is default.

`-v` Increase the debug level with 1, to provide more diagnostic messages. Can be added multiple times.

`file` The executable file to be loaded must be an SPARC or RISCV ELF file. On start-up, the file is loaded into the simulated memory.

3 Commands

Below is the description of commands that are recognized by the simulator. The command-line is parsed using GNU readline. A command history of 64 commands is maintained. Use the up/down arrows to recall previous commands. For more details, see the readline documentation.

`batch` *`file`*
: Execute a batch file of SIS commands.

`+bp` *`address`*
`break` *`address`*
: Set a breakpoint at *address*.

`bp`
: Print all breakpoints.

`delete` *`num`*
: Delete breakpoint *num*. Use `bp` or `break` to see which number is assigned to the breakpoints.

`csr`
: Show RISC-V CSR registers

`cont [`*`count`*`]`
: Continue execution at present position, optionally for *count* instructions.

`dis [`*`addr`*`] [`*`count`*`]`
: Disassemble [*count*] instructions at address [*addr*]. Default values for *count* is 16 and *addr* is the present program counter.

`echo` *`string`*
: Print *string* to the simulator window.

`float`
: Print the FPU registers

`gdb [`*`port`*`]`
: Start the gdb server interface. Default port is 1234, but can be overriden using the *port* argument. `gdb` should be started with `target extended-remote localhost:1234`.

`go` *`address`* `[`*`count`*`]`
: Set pc to *address* and resume execution. If *count* is given, `sis` will stop after *count* instructions have been executed.

`help`
: Print a small help menu for the SIS commands.

`hist [`*`trace_length`*`]`
: Enable the instruction trace buffer. The *trace_length* last executed instructions will be placed in the trace buffer. A `hist` command without a *trace_length* will display the trace buffer. Specifying a zero trace length will disable the trace buffer.

`load` *`file_name`*
: Load an ELF file into simulator memory.

`mem [addr] [count]`
: Display memory at [*addr*] for [*count*] bytes. Same default values as for the `dis` command.

`quit`
: Exits the simulator.

`perf [reset]`
: The `perf` command will display various execution statistics. A `perf reset` command will reset the statistics. This can be used if statistics shall be calculated only over a part of the program. The `run` and `reset` command also resets the statistic information.

`reg [reg_name] [value]`
: Print or set the CPU registers. `reg` without parameters prints the CPU registers. `reg` *reg_name value* sets the corresponding register to *value*. Valid register names for SPARC are psr, tbr, wim, y, g1-g7, o0-o7 and l0-l7. Valid register names for RISCV-V are mtvec, mstatus, pc, ra, sp, gp, tp, t0-t6, s0-s11 and a0-a7.

`reset`
: Perform a power-on reset. This command is equal to `run 0`.

`run [count]`
: Reset the simulator and start execution from the entry point of the loaded ELF file. If an instruction count is given (*count*), the simulator will stop after the specified number of instructions. The event queue is emptied but any set breakpoints remain.

`step`
: Execute one instruction and print it to the simulator console. Equal to command `trace 1`

`sym`
: List symbols and corresponding addresses in the loaded program.

`trace [count]`
: Resume the simulator at the present position and print each execute instruction executes. If an instruction count is given (*count*), the simulator will stop after the specified number of instructions.

`wmem addr data`
: Write *data* to memory at *addr*. Data is written as a 32-bit word.

`wp`
: Print all watchpoints

`+wpr address`
: Adds an read watchpoint at address <address>.

`-wpr num`
: Delete read watchpoint *num*. Use *wp* to see which number is assigned to the watchpoints.

`+wpw address`
`watch address`
: Adds an write watchpoint at *address*.

`-wpw` *num*

Delete write watchpoint *num*. Use `wp` to see which number is assigned to the watchpoints.

Typing a 'Ctrl-C' will interrupt a running simulator.

Short forms of the commands are allowed, e.g 'c' 'co' or 'con' are all interpreted as 'cont'.

4 Emulated Systems

`sis` is capable of emulating four different processor systems:

`ERC32` ERC32 SPARC V7 processor

`LEON2` LEON2 SPARC V8 processor

`LEON3` LEON3 SPARC V8 processor

`RISC-V` RISC-V (RV32IMACFD) processor

The following sections outline the emulation characteristics of the four supported systems.

4.1 ERC32 SPARC V7 processor

The radiation-hard ERC32 processor was developed by ESA in the mid-90's for critical space application. It was used in the control computer for the International Space Station (ISS) and also in the ATV re-supply ship for the ISS. The sub-sequent single-chip ERC32SC was used in a multitude of satellites, launchers and interplanetary probes, and is still being manufactured by Atmel. See the ESA ERC32 page (http://http://microelectronics.esa.int/erc32/index.html) for more technical documetation.

Sis emulates the original three-chip version of the ERC32 processor, consisting of the integer unit (IU), floating-point unit (FPU) and the memort controller (MEC). The IU is based on the Cypress CY601 SPARC V7 processor, while the FPU is based on the Meiko FPU. The MEC implements various peripheral functions and a memory controller. The single-chip verion of ERC32 (ERC32SC/TSC695F) is functionally identical to the original chip-set, but can operate at a higher frequency (25 MHz)

The following functions of the ERC32 are emulated by sis:

- IU & FPU with accurate timing
- UART A & B
- Real-time clock
- General purpose timer
- Interrupt controller
- Breakpoint register
- Watchpoint register
- 16 Mbyte ROM
- 16 Mbyte RAM

4.1.1 IU and FPU instruction timing.

The simulator provides cycle true simulation for ERC32. The following table shows the emulated instruction timing for IU & FPU:

Instruction	**Cycles**
jmpl, rett	2

load	2
store	3
load double	3
store double	4
other integer ops	1
fabs	2
fadds	4
faddd	4
fcmps	4
fcmpd	4
fdivs	20
fdivd	35
fmovs	2
fmuls	5
fmuld	9
fnegs	2
fsqrts	37
fsqrtd	65
fsubs	4
fsubd	4
fdtoi	7
fdots	3
fitos	6
fitod	6
fstoi	6
fstod	2

The parallel operation between the IU and FPU is modelled. This means that a FPU instruction will execute in parallel with other instructions as long as no data or resource dependency is detected. See the 90C602E data sheet for the various types of dependencies. Tracing using the 'trace' command will display the current simulator time in the left column. This time indicates when the instruction is fetched. If a dependency is detected, the following fetch will be delayed until the conflict is resolved.

The load dependency in the IU is also modelled - if the destination register of a load instruction is used by the following instruction, an idle cycle is inserted.

4.1.2 UART A and B

UART A is by default connected to the console, while UART B is disabled. Both UARTs can be connected to any file/device using the -uart1 and -uart2 options at start-up. The following registers are implemented:

Register	**Address**
UART A RX and TX register	0x01f800e0
UART B RX and TX register	0x01f800e4
UART status register	0x01f800e8

The UARTs generate interrupt 4 and 5 after each received or transmitted character. The error interrupt is generated if overflow occurs - other errors cannot occur.

4.1.3 Real-time clock and general purpose timer A

The following registers are implemented:

Register	Address
Real-time clock timer	0x01f80080
Real-time clock scaler program register	0x01f80084
Real-time clock counter program register	0x01f80080
General purpose timer	0x01f80088
Real-time clock scaler program register	0x01f8008c
General purpose timer counter register	0x01f80088
Timer control register	0x01f80098

4.1.4 Interrupt controller

The interrupt controller is implemented as in the MEC specification with the exception of the interrupt shape register. Since external interrupts are not possible, the interrupt shape register is not implemented. The only internal interrupts that are generated are the real-time clock, the general purpose timer and UARTs. However, all 15 interrupts can be tested via the interrupt force register.

The following registers are implemented:

Register	Address
Interrupt pending register	0x01f80048
Interrupt mask register	0x01f8004c
Interrupt clear register	0x01f80050
Interrupt force register	0x01f80054

4.1.5 System fault status registers

The system fault status register and fist failing address register are implemented and updated accordingly. Implemented registers are:

Register	Address
System fault status register	0x01f800a0
First failing address register	0x01f800a4

4.1.6 Memory interface

The following memory areas are valid for the ERC32 simulator:

Register	Address
0x00000000 - 0x01000000	ROM (16 Mbyte)
0x02000000 - 0x03000000	RAM (16 Mbyte)
0x01f80000 - 0x01f800ff	MEC registers

Access to unimplemented MEC registers or non-existing memory will result in a memory exception trap.

The memory configuration register is used to define available memory in the system. The fields RSIZ and PSIZ are used to set RAM and ROM size, the remaining fields are

not used. NOTE: after reset, the MEC is set to decode 4 Kbyte of ROM and 256 Kbyte of RAM. The memory configuration register has to be updated to reflect the available memory.

The waitstate configuration register is used to generate waitstates. This register must also be updated with the correct configuration after reset.

The memory protection scheme is implemented - it is enabled through bit 3 in the MEC control register.

The following registers are implemented:

Register	Address
MEC control register	0x01f80000
Memory control register	0x01f80010
Waitstate configuration register	0x01f80018
Memory access register 0	0x01f80020
Memory access register 1	0x01f80024

4.1.7 Watchdog

The watchdog is implemented as in the specification. The input clock is always the system clock regardless of WDCS bit in MEC configuration register.

The following registers are implemented:

Register	Address
Watchdog program/acknowledge register	0x01f80060
Watchdog trap door set register	0x01f80064

4.1.8 Software reset register

Implemented as in the specification (0x01f800004, write-only).

4.1.9 Power-down mode

The power-down register (0x01f800008) is implemented as in the specification. During power-down, the simulator skips time until next event in the event queue. Ctrl-C in the simulator window will exit the power-down mode.

4.1.10 MEC control register

The following bits are implemented in the MEC control register:

Bit	Name	Function
0	PRD	Power-down mode enable
1	SWR	Soft reset enable
2	APR	Access protection enable

4.2 LEON2 emulation

In LEON2 mode, SIS emulates a LEON2 system as defined in the LEON2 IP manual. The emulated system includes the LEON2 standard peripherals, 16 Mbyte ROM and 16 Mbyte RAM. The SPARC emulation supports an FPU but not the LEON2 MMU.

To start sis in LEON2 mode, use the -leon2 switch.

4.2.1 LEON2 peripherals

SIS emulates one LEON2 UART, the interrupt controller and the timer unit. The interrupt controller is implemented as described in the LEON2 IP manual, with the exception of the interrupt level register. Secondary interrupts are not supported. The timer unit is configured with two timers and separate interrupts (8 and 9). The scaler is configured to 16 bits, while the counters are 32 bits. The UART generates interrupt 3.

4.2.2 Memory interface

The following memory areas are valid for LEON2:

Address	Type
0x00000000 - 0x01000000	ROM (16 Mbyte)
0x40000000 - 0x41000000	RAM (16 Mbyte)
0x80000000 - 0x80000100	APB bus

Access to non-existing memory will result in a memory exception trap.

4.2.3 Power-down mode

The LEON2 power-down register (0x80000018) is supported. When power-down is entered, time is skipped forward until the next event in the event queue. A Ctrl-C in the simulator window will exit the power-down mode.

4.3 LEON3 emulation

In LEON3 mode, SIS emulates a LEON3 system as defined in the GRLIP IP manual. The emulated system includes the standard peripherals such as APBUART, GPTIMER, IRQMP and SRCTRL. The emulated system includes 16 Mbyte ROM and 16 Mbyte RAM. The SPARC emulation supports an FPU but not the LEON3 MMU.

To start sis in LEON3 mode, use the -leon3 switch.

4.3.1 LEON3 peripherals

The following IP cores from GRLIB are emulated in LEON3 mode:

IP Core	Address	Interrupt
APBMAST	0x80000000	-
APBUART	0x80000100	3
IRQMP	0x80000200	-
GPTIMER	0x80000300	8, 9

4.3.2 Memory interface

The following memory areas are valid for LEON3:

Address	Type
0x00000000 - 0x01000000	ROM (16 Mbyte)
0x40000000 - 0x41000000	RAM (16 Mbyte)
0x80000000 - 0x81000000	APB bus

0xFFFFF000 - 0xFFFFFFFF AHB plug&play

Access to non-existing memory will result in a memory exception trap.

4.3.3 Power-down mode

The LEON3 power-down register (%ars19) is supported. When power-down is entered, time is skipped forward until the next event in the event queue. A Ctrl-C in the simulator window will exit the power-down mode.

4.4 RISC-V emulation

In RISC-V mode, SIS emulates a RV32IMACFD processor as defined in the RISC-V specification 1.9. The RISC-V procssor is attached to an identical GRLIB sub-system as when LEON3 is emulated.

To start sis in RISC-V mode, use the -riscv switch.

4.4.1 Power-down mode

The RISC-V power-down feature (WFI) is supported. When power-down is entered, time is skipped forward until the next event in the event queue. Ctrl-C in the simulator window will exit the power-down mode.

4.4.2 Code coverage

Code coverage is currently only supported for 32-bit instructions, i.e. the C-extension can not be used when code coverage is measured.

4.4.3 RISC-V 64-bit timer

The standard RISC-V 64-bit timer is provided and can be read through the time and timeh CSR. The timer does not generare any interrupt and the timecmp register is not implemented.

5 Multi-processing

When emulating a LEON3 or RISC-V processor, SIS can emulate up to four cores in the target system (SMP). The cores are simulated in a round-robin fashion with a time-slice of 50 clocks. Shorter or longer time-slices can be selected using -d <clocks>.

To start SIS with SMP, use the switch -m <n> when starting the simulator where n can be 2 - 4.

6 Interfacing to GDB

SIS can be connected to gdb through a network socket using the gdb remote interface. Either start SIS with -gdb, or issue the 'gdb' command inside SIS, and connect gdb with 'target extended-remote localhost:1234'. The port can be changed using the -port option.

7 Code coverage

Code coverage data will be produce if sis is started with the -cov switch. The coverage data will be stored in a file name same as the file used with the load command, appended with .cov. For instance, if sis is run with hello.exe, the coverage data will be stored in hello.exe.cov. The coverage file is created when the simulator is exited.

The coverage file data consists of a starting address, and a number of coverage points indicating incremental 32-bit word addresses:

0x40000000 0 0 0 19 9 1 1 1 1 0 .....

The coverage points are in hexadecimal format. Bit 0 (lsb) indicates an executed instruction. Bit 3 indicates taken branch and bit 4 indicates an untaken branch. Bits 2 and 3 are currently not used.

For RISC-V, code coverage is only supported for 32-bit instructions, i.e. the C-extension can not be used when code coverage is measured.

8 Building SIS

SIS uses the GNU autoconf system, and can simply be build using `./configure` followed by `make`. To build a PDF version of the manual, do `make sis.pdf`.

The following custom configure options are recognized:

`-enable-l1cache`
: Enable the emulation of a L1 cache in multi-processor systems. Each core in an MP LEON3/RISC-V system will have a 4Kbyte instruction cache and a 4 Kbyte data cache. The cache only affects instruction timing, and has no effect on instruction behaviour.

Appendix A GNU Free Documentation License

Version 1.3, 3 November 2008

0. PREAMBLE

The purpose of this License is to make a manual, textbook, or other functional and useful document *free* in the sense of freedom: to assure everyone the effective freedom to copy and redistribute it, with or without modifying it, either commercially or non-commercially. Secondarily, this License preserves for the author and publisher a way to get credit for their work, while not being considered responsible for modifications made by others.

This License is a kind of "copyleft", which means that derivative works of the document must themselves be free in the same sense. It complements the GNU General Public License, which is a copyleft license designed for free software.

We have designed this License in order to use it for manuals for free software, because free software needs free documentation: a free program should come with manuals providing the same freedoms that the software does. But this License is not limited to software manuals; it can be used for any textual work, regardless of subject matter or whether it is published as a printed book. We recommend this License principally for works whose purpose is instruction or reference.

1. APPLICABILITY AND DEFINITIONS

This License applies to any manual or other work, in any medium, that contains a notice placed by the copyright holder saying it can be distributed under the terms of this License. Such a notice grants a world-wide, royalty-free license, unlimited in duration, to use that work under the conditions stated herein. The "Document", below, refers to any such manual or work. Any member of the public is a licensee, and is addressed as "you". You accept the license if you copy, modify or distribute the work in a way requiring permission under copyright law.

A "Modified Version" of the Document means any work containing the Document or a portion of it, either copied verbatim, or with modifications and/or translated into another language.

A "Secondary Section" is a named appendix or a front-matter section of the Document that deals exclusively with the relationship of the publishers or authors of the Document to the Document's overall subject (or to related matters) and contains nothing that could fall directly within that overall subject. (Thus, if the Document is in part a textbook of mathematics, a Secondary Section may not explain any mathematics.) The relationship could be a matter of historical connection with the subject or with related matters, or of legal, commercial, philosophical, ethical or political position regarding them.

The "Invariant Sections" are certain Secondary Sections whose titles are designated, as being those of Invariant Sections, in the notice that says that the Document is released

under this License. If a section does not fit the above definition of Secondary then it is not allowed to be designated as Invariant. The Document may contain zero Invariant Sections. If the Document does not identify any Invariant Sections then there are none.

The "Cover Texts" are certain short passages of text that are listed, as Front-Cover Texts or Back-Cover Texts, in the notice that says that the Document is released under this License. A Front-Cover Text may be at most 5 words, and a Back-Cover Text may be at most 25 words.

A "Transparent" copy of the Document means a machine-readable copy, represented in a format whose specification is available to the general public, that is suitable for revising the document straightforwardly with generic text editors or (for images composed of pixels) generic paint programs or (for drawings) some widely available drawing editor, and that is suitable for input to text formatters or for automatic translation to a variety of formats suitable for input to text formatters. A copy made in an otherwise Transparent file format whose markup, or absence of markup, has been arranged to thwart or discourage subsequent modification by readers is not Transparent. An image format is not Transparent if used for any substantial amount of text. A copy that is not "Transparent" is called "Opaque".

Examples of suitable formats for Transparent copies include plain ASCII without markup, Texinfo input format, LaTeX input format, SGML or XML using a publicly available DTD, and standard-conforming simple HTML, PostScript or PDF designed for human modification. Examples of transparent image formats include PNG, XCF and JPG. Opaque formats include proprietary formats that can be read and edited only by proprietary word processors, SGML or XML for which the DTD and/or processing tools are not generally available, and the machine-generated HTML, PostScript or PDF produced by some word processors for output purposes only.

The "Title Page" means, for a printed book, the title page itself, plus such following pages as are needed to hold, legibly, the material this License requires to appear in the title page. For works in formats which do not have any title page as such, "Title Page" means the text near the most prominent appearance of the work's title, preceding the beginning of the body of the text.

The "publisher" means any person or entity that distributes copies of the Document to the public.

A section "Entitled XYZ" means a named subunit of the Document whose title either is precisely XYZ or contains XYZ in parentheses following text that translates XYZ in another language. (Here XYZ stands for a specific section name mentioned below, such as "Acknowledgements", "Dedications", "Endorsements", or "History".) To "Preserve the Title" of such a section when you modify the Document means that it remains a section "Entitled XYZ" according to this definition.

The Document may include Warranty Disclaimers next to the notice which states that this License applies to the Document. These Warranty Disclaimers are considered to be included by reference in this License, but only as regards disclaiming warranties: any other implication that these Warranty Disclaimers may have is void and has no effect on the meaning of this License.

2. VERBATIM COPYING

You may copy and distribute the Document in any medium, either commercially or noncommercially, provided that this License, the copyright notices, and the license notice saying this License applies to the Document are reproduced in all copies, and that you add no other conditions whatsoever to those of this License. You may not use technical measures to obstruct or control the reading or further copying of the copies you make or distribute. However, you may accept compensation in exchange for copies. If you distribute a large enough number of copies you must also follow the conditions in section 3.

You may also lend copies, under the same conditions stated above, and you may publicly display copies.

3. COPYING IN QUANTITY

   If you publish printed copies (or copies in media that commonly have printed covers) of the Document, numbering more than 100, and the Document's license notice requires Cover Texts, you must enclose the copies in covers that carry, clearly and legibly, all these Cover Texts: Front-Cover Texts on the front cover, and Back-Cover Texts on the back cover. Both covers must also clearly and legibly identify you as the publisher of these copies. The front cover must present the full title with all words of the title equally prominent and visible. You may add other material on the covers in addition. Copying with changes limited to the covers, as long as they preserve the title of the Document and satisfy these conditions, can be treated as verbatim copying in other respects.

   If the required texts for either cover are too voluminous to fit legibly, you should put the first ones listed (as many as fit reasonably) on the actual cover, and continue the rest onto adjacent pages.

   If you publish or distribute Opaque copies of the Document numbering more than 100, you must either include a machine-readable Transparent copy along with each Opaque copy, or state in or with each Opaque copy a computer-network location from which the general network-using public has access to download using public-standard network protocols a complete Transparent copy of the Document, free of added material. If you use the latter option, you must take reasonably prudent steps, when you begin distribution of Opaque copies in quantity, to ensure that this Transparent copy will remain thus accessible at the stated location until at least one year after the last time you distribute an Opaque copy (directly or through your agents or retailers) of that edition to the public.

   It is requested, but not required, that you contact the authors of the Document well before redistributing any large number of copies, to give them a chance to provide you with an updated version of the Document.

4. MODIFICATIONS

   You may copy and distribute a Modified Version of the Document under the conditions of sections 2 and 3 above, provided that you release the Modified Version under precisely this License, with the Modified Version filling the role of the Document, thus licensing distribution and modification of the Modified Version to whoever possesses a copy of it. In addition, you must do these things in the Modified Version:

   A. Use in the Title Page (and on the covers, if any) a title distinct from that of the Document, and from those of previous versions (which should, if there were any,

be listed in the History section of the Document). You may use the same title as a previous version if the original publisher of that version gives permission.

B. List on the Title Page, as authors, one or more persons or entities responsible for authorship of the modifications in the Modified Version, together with at least five of the principal authors of the Document (all of its principal authors, if it has fewer than five), unless they release you from this requirement.

C. State on the Title page the name of the publisher of the Modified Version, as the publisher.

D. Preserve all the copyright notices of the Document.

E. Add an appropriate copyright notice for your modifications adjacent to the other copyright notices.

F. Include, immediately after the copyright notices, a license notice giving the public permission to use the Modified Version under the terms of this License, in the form shown in the Addendum below.

G. Preserve in that license notice the full lists of Invariant Sections and required Cover Texts given in the Document's license notice.

H. Include an unaltered copy of this License.

I. Preserve the section Entitled "History", Preserve its Title, and add to it an item stating at least the title, year, new authors, and publisher of the Modified Version as given on the Title Page. If there is no section Entitled "History" in the Document, create one stating the title, year, authors, and publisher of the Document as given on its Title Page, then add an item describing the Modified Version as stated in the previous sentence.

J. Preserve the network location, if any, given in the Document for public access to a Transparent copy of the Document, and likewise the network locations given in the Document for previous versions it was based on. These may be placed in the "History" section. You may omit a network location for a work that was published at least four years before the Document itself, or if the original publisher of the version it refers to gives permission.

K. For any section Entitled "Acknowledgements" or "Dedications", Preserve the Title of the section, and preserve in the section all the substance and tone of each of the contributor acknowledgements and/or dedications given therein.

L. Preserve all the Invariant Sections of the Document, unaltered in their text and in their titles. Section numbers or the equivalent are not considered part of the section titles.

M. Delete any section Entitled "Endorsements". Such a section may not be included in the Modified Version.

N. Do not retitle any existing section to be Entitled "Endorsements" or to conflict in title with any Invariant Section.

O. Preserve any Warranty Disclaimers.

If the Modified Version includes new front-matter sections or appendices that qualify as Secondary Sections and contain no material copied from the Document, you may at your option designate some or all of these sections as invariant. To do this, add their

titles to the list of Invariant Sections in the Modified Version's license notice. These titles must be distinct from any other section titles.

You may add a section Entitled "Endorsements", provided it contains nothing but endorsements of your Modified Version by various parties—for example, statements of peer review or that the text has been approved by an organization as the authoritative definition of a standard.

You may add a passage of up to five words as a Front-Cover Text, and a passage of up to 25 words as a Back-Cover Text, to the end of the list of Cover Texts in the Modified Version. Only one passage of Front-Cover Text and one of Back-Cover Text may be added by (or through arrangements made by) any one entity. If the Document already includes a cover text for the same cover, previously added by you or by arrangement made by the same entity you are acting on behalf of, you may not add another; but you may replace the old one, on explicit permission from the previous publisher that added the old one.

The author(s) and publisher(s) of the Document do not by this License give permission to use their names for publicity for or to assert or imply endorsement of any Modified Version.

5. COMBINING DOCUMENTS

   You may combine the Document with other documents released under this License, under the terms defined in section 4 above for modified versions, provided that you include in the combination all of the Invariant Sections of all of the original documents, unmodified, and list them all as Invariant Sections of your combined work in its license notice, and that you preserve all their Warranty Disclaimers.

   The combined work need only contain one copy of this License, and multiple identical Invariant Sections may be replaced with a single copy. If there are multiple Invariant Sections with the same name but different contents, make the title of each such section unique by adding at the end of it, in parentheses, the name of the original author or publisher of that section if known, or else a unique number. Make the same adjustment to the section titles in the list of Invariant Sections in the license notice of the combined work.

   In the combination, you must combine any sections Entitled "History" in the various original documents, forming one section Entitled "History"; likewise combine any sections Entitled "Acknowledgements", and any sections Entitled "Dedications". You must delete all sections Entitled "Endorsements."

6. COLLECTIONS OF DOCUMENTS

   You may make a collection consisting of the Document and other documents released under this License, and replace the individual copies of this License in the various documents with a single copy that is included in the collection, provided that you follow the rules of this License for verbatim copying of each of the documents in all other respects.

   You may extract a single document from such a collection, and distribute it individually under this License, provided you insert a copy of this License into the extracted document, and follow this License in all other respects regarding verbatim copying of that document.

7. AGGREGATION WITH INDEPENDENT WORKS

   A compilation of the Document or its derivatives with other separate and independent documents or works, in or on a volume of a storage or distribution medium, is called an "aggregate" if the copyright resulting from the compilation is not used to limit the legal rights of the compilation's users beyond what the individual works permit. When the Document is included in an aggregate, this License does not apply to the other works in the aggregate which are not themselves derivative works of the Document.

   If the Cover Text requirement of section 3 is applicable to these copies of the Document, then if the Document is less than one half of the entire aggregate, the Document's Cover Texts may be placed on covers that bracket the Document within the aggregate, or the electronic equivalent of covers if the Document is in electronic form. Otherwise they must appear on printed covers that bracket the whole aggregate.

8. TRANSLATION

   Translation is considered a kind of modification, so you may distribute translations of the Document under the terms of section 4. Replacing Invariant Sections with translations requires special permission from their copyright holders, but you may include translations of some or all Invariant Sections in addition to the original versions of these Invariant Sections. You may include a translation of this License, and all the license notices in the Document, and any Warranty Disclaimers, provided that you also include the original English version of this License and the original versions of those notices and disclaimers. In case of a disagreement between the translation and the original version of this License or a notice or disclaimer, the original version will prevail.

   If a section in the Document is Entitled "Acknowledgements", "Dedications", or "History", the requirement (section 4) to Preserve its Title (section 1) will typically require changing the actual title.

9. TERMINATION

   You may not copy, modify, sublicense, or distribute the Document except as expressly provided under this License. Any attempt otherwise to copy, modify, sublicense, or distribute it is void, and will automatically terminate your rights under this License.

   However, if you cease all violation of this License, then your license from a particular copyright holder is reinstated (a) provisionally, unless and until the copyright holder explicitly and finally terminates your license, and (b) permanently, if the copyright holder fails to notify you of the violation by some reasonable means prior to 60 days after the cessation.

   Moreover, your license from a particular copyright holder is reinstated permanently if the copyright holder notifies you of the violation by some reasonable means, this is the first time you have received notice of violation of this License (for any work) from that copyright holder, and you cure the violation prior to 30 days after your receipt of the notice.

   Termination of your rights under this section does not terminate the licenses of parties who have received copies or rights from you under this License. If your rights have been terminated and not permanently reinstated, receipt of a copy of some or all of the same material does not give you any rights to use it.

10. FUTURE REVISIONS OF THIS LICENSE

    The Free Software Foundation may publish new, revised versions of the GNU Free Documentation License from time to time. Such new versions will be similar in spirit to the present version, but may differ in detail to address new problems or concerns. See http://www.gnu.org/copyleft/.

    Each version of the License is given a distinguishing version number. If the Document specifies that a particular numbered version of this License "or any later version" applies to it, you have the option of following the terms and conditions either of that specified version or of any later version that has been published (not as a draft) by the Free Software Foundation. If the Document does not specify a version number of this License, you may choose any version ever published (not as a draft) by the Free Software Foundation. If the Document specifies that a proxy can decide which future versions of this License can be used, that proxy's public statement of acceptance of a version permanently authorizes you to choose that version for the Document.

11. RELICENSING

    "Massive Multiauthor Collaboration Site" (or "MMC Site") means any World Wide Web server that publishes copyrightable works and also provides prominent facilities for anybody to edit those works. A public wiki that anybody can edit is an example of such a server. A "Massive Multiauthor Collaboration" (or "MMC") contained in the site means any set of copyrightable works thus published on the MMC site.

    "CC-BY-SA" means the Creative Commons Attribution-Share Alike 3.0 license published by Creative Commons Corporation, a not-for-profit corporation with a principal place of business in San Francisco, California, as well as future copyleft versions of that license published by that same organization.

    "Incorporate" means to publish or republish a Document, in whole or in part, as part of another Document.

    An MMC is "eligible for relicensing" if it is licensed under this License, and if all works that were first published under this License somewhere other than this MMC, and subsequently incorporated in whole or in part into the MMC, (1) had no cover texts or invariant sections, and (2) were thus incorporated prior to November 1, 2008.

    The operator of an MMC Site may republish an MMC contained in the site under CC-BY-SA on the same site at any time before August 1, 2009, provided the MMC is eligible for relicensing.

ADDENDUM: How to use this License for your documents

To use this License in a document you have written, include a copy of the License in the document and put the following copyright and license notices just after the title page:

```
Copyright (C)  year  your name.
Permission is granted to copy, distribute and/or modify this document
under the terms of the GNU Free Documentation License, Version 1.3
or any later version published by the Free Software Foundation;
with no Invariant Sections, no Front-Cover Texts, and no Back-Cover
Texts.  A copy of the license is included in the section entitled ``GNU
Free Documentation License''.
```

If you have Invariant Sections, Front-Cover Texts and Back-Cover Texts, replace the "with. . .Texts." line with this:

```
with the Invariant Sections being list their titles, with
the Front-Cover Texts being list, and with the Back-Cover Texts
being list.
```

If you have Invariant Sections without Cover Texts, or some other combination of the three, merge those two alternatives to suit the situation.

If your document contains nontrivial examples of program code, we recommend releasing these examples in parallel under your choice of free software license, such as the GNU General Public License, to permit their use in free software.

Index

B

Building SIS 15

C

Code coverage 14
Commands 3

E

Emulated Systems 6

I

Interfacing to GDB 13
Introduction 1
invoking `sis` 2

M

Multi-processing 12

S

`sis` 2