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1 Introduction

SIS is a SPARC V7/V8 and RISC-V RV32IMACFD architecture simulator. It consists of three main parts: an event-based simulator core, a CPU (SPARC/RISCV) emulation module and system-specific memory and peripheral modules.

SIS can emulate four specific systems:

- **ERC32**  ERC32 SPARC V7 processor
- **LEON2**  LEON2 SPARC V8 processor
- **LEON3**  LEON3 SPARC V8 processor
- **RISC-V** RISC-V (RV32IMACFD) processor

The LEON3 and RISC-V emulation also supports SMP with up to four processor cores.
2 Invoking sis

The simulator is started as follows:

    sis [options] [file]

The following options are recognized:

- **-c file**  Read sis commands from file at startup.
- **-cov**    Enable code coverage and write a coverage file at exit.
- **-d clocks**  Set the number of clocks in each time-slice for multi-processor simulation. Default is 50, set lower for higher accuracy.
- **-erc32**  Emulate the SPARC V7 ERC32 processor
- **-freq freq**  Set frequency of emulated cpu. This is used by the ‘perf’ command to calculated the MIPS figure for a particular configuration. The frequency must be an integer indicating the frequency in MHz.
- **-gdb**    Start a gdb server, listening on port 1234. An alternative port can be specified with -port nn.
- **-leon2**  Emulate the SPARC V8 LEON2 processor
- **-leon3**  Emulate the SPARC V8 LEON3 processor
- **-m cores**  Enable the number of cores (2 - 4) in a leon3 or RISC-V multi-processor system.
- **-nfp**    Disable the simulated FPU, so each FPU instruction will generate a FPU disabled trap.
- **-port port**  Use port for the gdb server. Default is port 1234.
- **-r**    Start execution immediately without an interactive shell. This is useful for automated testing.
- **-riscv**  Emulate a RISC-V RV32IMACFD processor
- **-tlim delay**  Used together with -r to limit the amount of simulated time that the simulator runs for before exiting. The following units are recognized: us, ms and s. To limit simulated time to 100 seconds, use: -tlim 100 s.
- **-uart1 device**  Connect UART1 (console) of the simulator to device. stdin/stout is default.
- **-v**    Increase the debug level with 1, to provide more diagnostic messages. Can be added multiple times.

**file**  The executable file to be loaded must be an SPARC or RISCV ELF file. On start-up, the file is loaded into the simulated memory.
3 Commands

Below is the description of commands that are recognized by the simulator. The command-line is parsed using GNU readline. A command history of 64 commands is maintained. Use the up/down arrows to recall previous commands. For more details, see the readline documentation.

batch file
Execute a batch file of SIS commands.

+bp address
break address
Set a breakpoint at address.

bp
Print all breakpoints.

delete num
Delete breakpoint num. Use bp or break to see which number is assigned to the breakpoints.

csr
Show RISC-V CSR registers

cont [count]
Continue execution at present position, optionally for count instructions.

dis [addr] [count]
Disassemble [count] instructions at address [addr]. Default values for count is 16 and addr is the present program counter.

echo string
Print string to the simulator window.

float
Print the FPU registers

gdb [port]
Start the gdb server interface. Default port is 1234, but can be overridden using the port argument. gdb should be started with target extended-remote localhost:1234.

go address [count]
Set pc to address and resume execution. If count is given, sis will stop after count instructions have been executed.

help
Print a small help menu for the SIS commands.

hist [trace_length]
Enable the instruction trace buffer. The trace_length last executed instructions will be placed in the trace buffer. A hist command without a trace_length will display the trace buffer. Specifying a zero trace length will disable the trace buffer.

load file_name
Load an ELF file into simulator memory.
Chapter 3: Commands

mem [addr] [count]
Display memory at [addr] for [count] bytes. Same default values as for the dis command.

quit
Exits the simulator.

perf [reset]
The perf command will display various execution statistics. A perf reset command will reset the statistics. This can be used if statistics shall be calculated only over a part of the program. The run and reset command also resets the statistic information.

reg [reg_name] [value]
Print or set the CPU registers. reg without parameters prints the CPU registers. reg reg_name value sets the corresponding register to value. Valid register names for SPARC are psr, tbr, wim, y, g1-g7, o0-o7 and l0-l7. Valid register names for RISCV-V are mtvec, mstatus, pc, ra, sp, gp, tp, t0-t6, s0-s11 and a0-a7.

reset
Perform a power-on reset. This command is equal to run 0.

run [count]
Reset the simulator and start execution from the entry point of the loaded ELF file. If an instruction count is given (count), the simulator will stop after the specified number of instructions. The event queue is emptied but any set breakpoints remain.

step
Execute one instruction and print it to the simulator console. Equal to command trace 1

sym
List symbols and corresponding addresses in the loaded program.

trace [count]
Resume the simulator at the present position and print each execute instruction executes. If an instruction count is given (count), the simulator will stop after the specified number of instructions.

wmem addr data
Write data to memory at addr. Data is written as a 32-bit word.

wp
Print all watchpoints

+wpr address
Adds an read watchpoint at address <address>.

-wpr num
Delete read watchpoint num. Use wp to see which number is assigned to the watchpoints.

+wpw address
watch address
Adds an write watchpoint at address.
Command: *-wp* `num`

Delete write watchpoint `num`. Use `wp` to see which number is assigned to the watchpoints.

Typing a 'Ctrl-C' will interrupt a running simulator.

Short forms of the commands are allowed, e.g 'c' 'co' or 'con' are all interpreted as 'cont'.
Chapter 4: Emulated Systems

sis is capable of emulating four different processor systems:

**ERC32**  ERC32 SPARC V7 processor
**LEON2**  LEON2 SPARC V8 processor
**LEON3**  LEON3 SPARC V8 processor
**RISC-V** RISC-V (RV32IMACFD) processor

The following sections outline the emulation characteristics of the four supported systems.

### 4.1 ERC32 SPARC V7 processor

The radiation-hard ERC32 processor was developed by ESA in the mid-90’s for critical space application. It was used in the control computer for the International Space Station (ISS) and also in the ATV re-supply ship for the ISS. The subsequent single-chip ERC32SC was used in a multitude of satellites, launchers and inter-planetary probes, and is still being manufactured by Atmel. See the ESA ERC32 page (http://microelectronics.esa.int/erc32/index.html) for more technical documentation.

Sis emulates the original three-chip version of the ERC32 processor, consisting of the integer unit (IU), floating-point unit (FPU) and the memory controller (MEC). The IU is based on the Cypress CY601 SPARC V7 processor, while the FPU is based on the Meiko FPU. The MEC implements various peripheral functions and a memory controller. The single-chip version of ERC32 (ERC32SC/TSC695F) is functionally identical to the original chip-set, but can operate at a higher frequency (25 MHz)

The following functions of the ERC32 are emulated by sis:

- IU & FPU with accurate timing
- UART A & B
- Real-time clock
- General purpose timer
- Interrupt controller
- Breakpoint register
- Watchpoint register
- 16 Mbyte ROM
- 16 Mbyte RAM

#### 4.1.1 IU and FPU instruction timing.

The simulator provides cycle true simulation for ERC32. The following table shows the emulated instruction timing for IU & FPU:

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Cycles</th>
</tr>
</thead>
<tbody>
<tr>
<td>jmpl, rett</td>
<td>2</td>
</tr>
</tbody>
</table>
load  2
store  3
load double  3
store double  4
other integer ops  1
fabs  2
fadds  4
fadd  4
fcmps  4
fcmpd  4
fdivs  20
fdivd  35
fmovs  2
fmuls  5
fmuld  9
fnegs  2
fsqrts  37
fsqrtld  65
fsubs  4
fsubd  4
fdtou  7
fdots  3
fitos  6
fitod  6
fstoi  6
fstod  2

The parallel operation between the IU and FPU is modelled. This means that a FPU instruction will execute in parallel with other instructions as long as no data or resource dependency is detected. See the 90C602E data sheet for the various types of dependencies. Tracing using the 'trace' command will display the current simulator time in the left column. This time indicates when the instruction is fetched. If a dependency is detected, the following fetch will be delayed until the conflict is resolved.

The load dependency in the IU is also modelled - if the destination register of a load instruction is used by the following instruction, an idle cycle is inserted.

### 4.1.2 UART A and B

UART A is by default connected to the console, while UART B is disabled. Both UARTs can be connected to any file/device using the -uart1 and -uart2 options at start-up. The following registers are implemented:

<table>
<thead>
<tr>
<th>Register</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>UART A RX and TX register</td>
<td>0x01f800e0</td>
</tr>
<tr>
<td>UART B RX and TX register</td>
<td>0x01f800e4</td>
</tr>
<tr>
<td>UART status register</td>
<td>0x01f800e8</td>
</tr>
</tbody>
</table>

The UARTs generate interrupt 4 and 5 after each received or transmitted character. The error interrupt is generated if overflow occurs - other errors cannot occur.
4.1.3 Real-time clock and general purpose timer A

The following registers are implemented:

<table>
<thead>
<tr>
<th>Register</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>Real-time clock timer</td>
<td>0x01f80080</td>
</tr>
<tr>
<td>Real-time clock scaler program register</td>
<td>0x01f80084</td>
</tr>
<tr>
<td>Real-time clock counter program register</td>
<td>0x01f80080</td>
</tr>
<tr>
<td>General purpose timer</td>
<td>0x01f80088</td>
</tr>
<tr>
<td>Real-time clock scaler program register</td>
<td>0x01f8008c</td>
</tr>
<tr>
<td>General purpose timer counter register</td>
<td>0x01f80088</td>
</tr>
<tr>
<td>Timer control register</td>
<td>0x01f80098</td>
</tr>
</tbody>
</table>

4.1.4 Interrupt controller

The interrupt controller is implemented as in the MEC specification with the exception of the interrupt shape register. Since external interrupts are not possible, the interrupt shape register is not implemented. The only internal interrupts that are generated are the real-time clock, the general purpose timer and UARTs. However, all 15 interrupts can be tested via the interrupt force register.

The following registers are implemented:

<table>
<thead>
<tr>
<th>Register</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interrupt pending register</td>
<td>0x01f80048</td>
</tr>
<tr>
<td>Interrupt mask register</td>
<td>0x01f8004c</td>
</tr>
<tr>
<td>Interrupt clear register</td>
<td>0x01f80050</td>
</tr>
<tr>
<td>Interrupt force register</td>
<td>0x01f80054</td>
</tr>
</tbody>
</table>

4.1.5 System fault status registers

The system fault status register and first failing address register are implemented and updated accordingly. Implemented registers are:

<table>
<thead>
<tr>
<th>Register</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>System fault status register</td>
<td>0x01f800a0</td>
</tr>
<tr>
<td>First failing address register</td>
<td>0x01f800a4</td>
</tr>
</tbody>
</table>

4.1.6 Memory interface

The following memory areas are valid for the ERC32 simulator:

<table>
<thead>
<tr>
<th>Register</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x000000000 - 0x01000000</td>
<td>ROM (16 Mbyte)</td>
</tr>
<tr>
<td>0x020000000 - 0x03000000</td>
<td>RAM (16 Mbyte)</td>
</tr>
<tr>
<td>0x01f800000 - 0x01f800ff</td>
<td>MEC registers</td>
</tr>
</tbody>
</table>

Access to unimplemented MEC registers or non-existing memory will result in a memory exception trap.

The memory configuration register is used to define available memory in the system. The fields RSIZ and PSIZ are used to set RAM and ROM size, the remaining fields are
not used. NOTE: after reset, the MEC is set to decode 4 Kbyte of ROM and 256 Kbyte of RAM. The memory configuration register has to be updated to reflect the available memory.

The waitstate configuration register is used to generate waitstates. This register must also be updated with the correct configuration after reset.

The memory protection scheme is implemented - it is enabled through bit 3 in the MEC control register.

The following registers are implemented:

<table>
<thead>
<tr>
<th>Register</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>MEC control register</td>
<td>0x01f80000</td>
</tr>
<tr>
<td>Memory control register</td>
<td>0x01f80010</td>
</tr>
<tr>
<td>Waitstate configuration register</td>
<td>0x01f80018</td>
</tr>
<tr>
<td>Memory access register 0</td>
<td>0x01f80020</td>
</tr>
<tr>
<td>Memory access register 1</td>
<td>0x01f80024</td>
</tr>
</tbody>
</table>

### 4.1.7 Watchdog

The watchdog is implemented as in the specification. The input clock is always the system clock regardless of WDCS bit in MEC configuration register.

The following registers are implemented:

<table>
<thead>
<tr>
<th>Register</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>Watchdog program/acknowledge register</td>
<td>0x01f80060</td>
</tr>
<tr>
<td>Watchdog trap door set register</td>
<td>0x01f80064</td>
</tr>
</tbody>
</table>

### 4.1.8 Software reset register

Implemented as in the specification (0x01f800004, write-only).

### 4.1.9 Power-down mode

The power-down register (0x01f800008) is implemented as in the specification. During power-down, the simulator skips time until next event in the event queue. Ctrl-C in the simulator window will exit the power-down mode.

### 4.1.10 MEC control register

The following bits are implemented in the MEC control register:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>PRD</td>
<td>Power-down mode enable</td>
</tr>
<tr>
<td>1</td>
<td>SWR</td>
<td>Soft reset enable</td>
</tr>
<tr>
<td>2</td>
<td>APR</td>
<td>Access protection enable</td>
</tr>
</tbody>
</table>

### 4.2 LEON2 emulation

In LEON2 mode, SIS emulates a LEON2 system as defined in the LEON2 IP manual. The emulated system includes the LEON2 standard peripherals, 16 Mbyte ROM and 16 Mbyte RAM. The SPARC emulation supports an FPU but not the LEON2 MMU.

To start sis in LEON2 mode, use the -leon2 switch.


4.2.1 LEON2 peripherals
SIS emulates one LEON2 UART, the interrupt controller and the timer unit. The interrupt controller is implemented as described in the LEON2 IP manual, with the exception of the interrupt level register. Secondary interrupts are not supported. The timer unit is configured with two timers and separate interrupts (8 and 9). The scaler is configured to 16 bits, while the counters are 32 bits. The UART generates interrupt 3.

4.2.2 Memory interface
The following memory areas are valid for LEON2:

<table>
<thead>
<tr>
<th>Address</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00000000 - 0x01000000</td>
<td>ROM (16 Mbyte)</td>
</tr>
<tr>
<td>0x40000000 - 0x41000000</td>
<td>RAM (16 Mbyte)</td>
</tr>
<tr>
<td>0x80000000 - 0x80000100</td>
<td>APB bus</td>
</tr>
</tbody>
</table>

Access to non-existing memory will result in a memory exception trap.

4.2.3 Power-down mode
The LEON2 power-down register (0x80000018) is supported. When power-down is entered, time is skipped forward until the next event in the event queue. A Ctrl-C in the simulator window will exit the power-down mode.

4.3 LEON3 emulation
In LEON3 mode, SIS emulates a LEON3 system as defined in the GRLIP IP manual. The emulated system includes the standard peripherals such as APBUART, GPTIMER, IRQMP and SRCTRL. The emulated system includes 16 Mbyte ROM and 16 Mbyte RAM. The SPARC emulation supports an FPU but not the LEON3 MMU.

To start sis in LEON3 mode, use the -leon3 switch.

4.3.1 LEON3 peripherals
The following IP cores from GRLIB are emulated in LEON3 mode:

<table>
<thead>
<tr>
<th>IP Core</th>
<th>Address</th>
<th>Interrupt</th>
</tr>
</thead>
<tbody>
<tr>
<td>APBMAST</td>
<td>0x80000000</td>
<td>-</td>
</tr>
<tr>
<td>APBUART</td>
<td>0x80000100</td>
<td>3</td>
</tr>
<tr>
<td>IRQMP</td>
<td>0x80000200</td>
<td>-</td>
</tr>
<tr>
<td>GPTIMER</td>
<td>0x80000300</td>
<td>8, 9</td>
</tr>
</tbody>
</table>

4.3.2 Memory interface
The following memory areas are valid for LEON3:

<table>
<thead>
<tr>
<th>Address</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00000000 - 0x01000000</td>
<td>ROM (16 Mbyte)</td>
</tr>
<tr>
<td>0x40000000 - 0x41000000</td>
<td>RAM (16 Mbyte)</td>
</tr>
<tr>
<td>0x80000000 - 0x81000000</td>
<td>APB bus</td>
</tr>
</tbody>
</table>
0xFFFFF000 - 0xFFFFFFFF AHB plug&play

Access to non-existing memory will result in a memory exception trap.

4.3.3 Power-down mode
The LEON3 power-down register (%ars19) is supported. When power-down is entered, time is skipped forward until the next event in the event queue. A Ctrl-C in the simulator window will exit the power-down mode.

4.4 RISC-V emulation
In RISC-V mode, SIS emulates a RV32IMACFD processor as defined in the RISC-V specification 1.9. The RISC-V processor is attached to an identical GRLIB sub-system as when LEON3 is emulated.

To start sis in RISC-V mode, use the -riscv switch.

4.4.1 Power-down mode
The RISC-V power-down feature (WFI) is supported. When power-down is entered, time is skipped forward until the next event in the event queue. Ctrl-C in the simulator window will exit the power-down mode.

4.4.2 Code coverage
Code coverage is currently only supported for 32-bit instructions, i.e. the C-extension can not be used when code coverage is measured.

4.4.3 RISC-V 64-bit timer
The standard RISC-V 64-bit timer is provided and can be read through the time and timeh CSR. The timer does not generate any interrupt and the timecmp register is not implemented.
5 Multi-processing

When emulating a LEON3 or RISC-V processor, SIS can emulate up to four cores in the target system (SMP). The cores are simulated in a round-robin fashion with a time-slice of 50 clocks. Shorter or longer time-slices can be selected using -d <clocks>.

To start SIS with SMP, use the switch -m <n> when starting the simulator where n can be 2 - 4.
6 Interfacing to GDB

SIS can be connected to gdb through a network socket using the gdb remote interface. Either start SIS with -gdb, or issue the 'gdb' command inside SIS, and connect gdb with 'target extended-remote localhost:1234'. The port can be changed using the -port option.
Chapter 7: Code coverage

7 Code coverage

Code coverage data will be produce if sis is started with the -cov switch. The coverage data will be stored in a file name same as the file used with the load command, appended with .cov. For instance, if sis is run with hello.exe, the coverage data will be stored in hello.exe.cov. The coverage file is created when the simulator is exited.

The coverage file data consists of a starting address, and a number of coverage points indicating incremental 32-bit word addresses:

0x40000000 0 0 0 1 9 1 1 1 1 1 0 ....

The coverage points are in hexadecimal format. Bit 0 (lsb) indicates an executed instruction. Bit 3 indicates taken branch and bit 4 indicates an untaken branch. Bits 2 and 3 are currently not used.

For RISC-V, code coverage is only supported for 32-bit instructions, i.e. the C-extension can not be used when code coverage is measured.
8 Building SIS

SIS uses the GNU autoconf system, and can simply be build using 

```
./configure
```

followed by `make`. To build a PDF version of the manual, do `make sis.pdf`.

The following custom configure options are recognized:

- **-enable-l1cache**
  
  Enable the emulation of a L1 cache in multi-processor systems. Each core in an MP LEON3/RISC-V system will have a 4Kbyte instruction cache and a 4 Kbyte data cache. The cache only affects instruction timing, and has no effect on instruction behaviour.
Appendix A GNU Free Documentation License

Version 1.3, 3 November 2008

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